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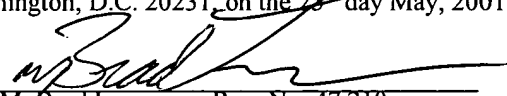
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Kevin Frazier, et al.  
Serial No: 09/730,453  
Filed: December 5, 2000  
For: MULTI-PROTOCOL PACKET TRANSLATOR  
Examiner: Not yet assigned  
Art Unit: 2661

#6/B  
L. McLauchlin  
8-7-01

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

The undersigned hereby certifies that this document is being placed in the United States mail with first-class postage attached, addressed to Commissioner for Patents, Washington, D.C. 20231, on the 25<sup>th</sup> day May, 2001.

  
M. Brad Lawrence, Reg. No. 47,210

Commissioner for Patents  
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

In response to the NOTICE TO FILE CORRECTED APPLICATION PAPERS mailed March 14, 2001, please amend the above-identified application as follows:

In the Specification:

Please replace the paragraph beginning at line 1 of page 5 as shown.

FIG. 13 illustrates a next step in translating the packet of FIG. 7A into the packet of FIG. 7B, using the circuit of FIG. 10;

Please replace the paragraph beginning at line 3 of page 27 as shown.

FIG. 13 illustrates the next step in the translation. At this point, the two most significant bytes for the ElanID field are stored in a four byte word in the information memory 101b, as shown. These two bytes cannot be written directly to the output memory, however, because the output memory requires a four byte word to be written. Accordingly, the two bytes of the ElanID need to be stored in the storage alignment units 103, for later writing to the output memory 105. This is done as illustrated in FIG. 13. During this clock cycle, no information is